REMARKS

After entry of the foregoing amendments, claims 2-26 are pending in the application and are presented for reconsideration and further examination in view of the foregoing amendments and the following remarks. By the foregoing amendments, claim 1 and 6 have been cancelled without prejudice or disclaimer, claims 2, 4, 5, 7, 9, 10, 11, 12, 15, and 21 have been amended and new claim 26 has been added.

Interview Summary

The undersigned thanks the Examiner for the courtesy extended during the interview conducted on February 26, 2008. During the interview the use of the switching signal to generate, at the butterfly module, a control signal for the multiplier was discussed in view of Yeh's more complex control circuit which is not located at the butterfly module and does not generate control of the multiplier from the current and past states of the switching signal. The rejection under §101 was also discussed.

35 U.S.C. §112

In the office action claims 1-25 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to comply with the enablement requirement.

In particular, the language "the control signal comprising a combination of a current and a prior switching signal" in claims 1, 12, 15 and 21 was objected to as being new subject matter. Applicant respectfully traverses this rejection.

The subject matter of the cited language was described in the application as filed. For example, FIG. 12 illustrates a control signal provided by a control circuitry, for example a logical AND gate 188, receiving as its input, a current switching signal S_n and a prior switching signal S_{n-1} (see, paragraph 45 at the top of page 16). Therefore, withdrawal of the rejection under §112 is respectfully requested.

35 U.S.C. §101

Claims 1-25 were rejected under 35 U.S.C. 101 on the grounds that the claimed invention is directed to non-statutory subject matter. Applicant respectfully traverses this ground of rejection.

According to the requirement of section 101, "whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter... may obtain a patent". With regards to the apparatus claims, they are directed to a FFT processor which is at least a machine and is therefore patentable subject matter. Similarly, the method claims are directed to a "method of performing an FFT on a data sequence of *N* samples in an FFT processor having a butterfly module" which is a useful process.

The Examiner further stated that "there is no cited limitation in the claims that breathes sufficient life and meaning into the preamble so as to limit it to a particular practical application rather than being so broad and sweeping as to cover every substantial practical application of the idea embodied therein". According to the guidelines of the MPEP the examiner must show "why the claimed invention would impermissibly cover every substantial practical application of, and thereby preempt all use of, an abstract idea, natural phenomenon, or law of nature." Applicant respectfully submits that no such showing has been made.

Each of the pending claims (as amended) includes language regarding specific switching signals and control circuitry which are used to generate a control signal for a selectable multiplier. For example, new claim 26 states in part, "control circuitry configured to generate the first control signal in response to the current state of the second switching signal and the prior state of the second switching signal." Clearly, the current claims do not preempt all use of an abstract idea or law of nature. Rather, they are directed to an improved circuit for an FFT processor.

Withdrawal of the rejection under §101 is respectfully requested.

35 U.S.C. §102(e)

Claims 1-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Yeh (US

Publication No. 2004/0059766). Yeh does not anticipate the amended claims. Applicant reserves the right to challenge whether Yeh is available as prior art against the present application. New claim 26 represents cancelled claim 1 rewritten and amended.

Claim 26 is directed to a pipelined FFT processor which includes a series of butterfly modules and selectable multipliers. Each selectable multiplier has an associated control circuit in the following butterfly module which generates the control signal which controls the operation of the selectable multiplier. The control circuit generates the control signal from the current and previous states of the switching signal which controls the operation of the butterfly module. Therefore, control of the FFT processor is simplified because a single switching signal (per butterfly module) is generated and used to control the butterfly module and is also used to generate, at the butterfly module, the signal to control the selectable multiplier. This results in fewer signals being routed from a processor controller which leads to a more compact and efficient processor circuit. Additionally, in one embodiment the design is easier to scale up (more butterfly modules) because only a single switching signal has to be added for each additional butterfly module.

Yeh does not teach or suggest such a FFT processor. For example, in connection with Figure 5, Yeh describes three control lines (signals) 206a, b, and c going to the butterfly unit from the control unit 36. 206c appears to control the output of the complex rotator 208. That control signal is not generated by control circuitry at the butterfly unit and does not appear to be generated from the current and past state of a switching signal. Therefore, Yeh must route more control signals per butterfly unit (three are shown in figure 5) which would lead to a larger and less efficient processor circuit.

Similarly, independent claim 12 is directed to a FFT processor having a series of FFT stage modules having, for example, a selectable multiplier which is "selected in response to a first control signal provided by a first control circuitry with the second FFT stage module, the first control signal comprising a combination of a current and a prior switching signal, and a second stage radix-2 butterfly unit for controlled by the switching signal." (emphasis added) Yeh does not teach or suggest such a FFT processor. As was described above, Yeh does not teach or suggest such a FFT processor.

Independent claim 15 is directed to a FFT processor having second and third stage FFT modules wherein, for example, "a selectable multiplier is selected in response to a first control signal provided with the second FFT stage module, the first control signal comprising a combination of a current and a prior switching signal, and a second stage radix-2 butterfly unit responsive to the current switching signal for providing a second stage output sequence in accordance with the butterfly operation performed on the output of the selectable multiplier." (emphasis added). Yeh does not teach or suggest such a FFT processor for at least the reasons set forth above.

Independent claim 21 is directed to a method of performing an FFT on a data sequence of N samples in an FFT processor having a butterfly module. The claimed method includes, "selectively multiplying the generated 2-point FFT sequence by a complex valued multiplicand, wherein a multiplier for selectively multiplying is selected in response to a control signal provided with each butterfly module, the control signal comprising a combination of a current and a prior switching signal." Yeh does not teach or suggest the claimed method. For example, as was noted above, Yeh does not teach controlling a multiplier with a control signal which comprises a combination of the current and prior switching signal.

Therefore, applicant respectfully submits that each of the pending claims is patentable over Yeh.

CONCLUSION

The Applicant has endeavored to address all of the Examiner's concerns as expressed in the outstanding Office Action. Accordingly, amendments to the claims, the reasons therefor, and arguments in support of the patentability of the pending claim set are presented above. Any claim amendments which are not specifically discussed in the above remarks are made in order to improve the clarity of claim language, to correct grammatical mistakes or ambiguities, and to otherwise improve the capacity of the claims to particularly and distinctly point out the invention to those of skill in the art. In light of the above amendments and remarks, reconsideration and withdrawal of the outstanding rejections is specifically requested. If the Examiner finds any remaining impediment to the prompt allowance of these claims that could be clarified with a telephone conference, the Examiner is respectfully requested to initiate the same with the undersigned.

Respectfully submitted,

Dated: 4/10/08

Richard E. Campbell
Registration No. 34,790
Attorney of Record

Procopio, Cory, Hargreaves & Savitch LLP
530 B Street, Suite 2100
San Diego, CA 92101
Telephone: 619-238-1900
Fax: 619-235-0398
Customer No. 27189